Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A test method of a memory IC function, comprising ~~the following steps of~~:

preparing a memory tester;

preparing memory ICs of different types;

transmitting data related to each test method of the [[these]] memory ICs to the memory tester;

generating a random number indicative of a period of time;

executing a test of a predetermined memory IC for the period of time in accordance with ~~in reply to~~ the generated random number; [[and]]

judging whether [[the]] tests of all the memory ICs are finished or not[[:]];

repeating said generating a ~~the generation of the~~ random number and said executing a ~~the execution of the~~ test if tests of all the memory ICs ~~when they~~ are not finished; and

ending ~~finishing the~~ processing if tests of all the memory ICs ~~when they~~ are finished.

Claim 2 (Currently Amended): The test method of a memory IC function, according to Claim 1, wherein the random number is an arbitrary integer from 0 to 255.

Claim 3 (Currently Amended): The test method of a memory IC function, according to Claim 1, wherein the memory ~~IC includes~~ ICs include Flash ROM, DRAM, and SDRAM.

Claim 4 (Currently Amended): The test method of a memory IC function, according to Claim 1, further comprising ~~a step of~~ performing timer interruption processing after said executing a test ~~execution of the test of the memory IC~~.

Claim 5 (Original): The test method of a memory IC function, according to Claim 4, wherein the timer interruption processing is performed with a predetermined cycle.

Claim 6 (Currently Amended): The test method of a memory IC function, according to Claim 5, wherein the predetermined cycle is in a range of milliseconds ~~defined by the millisecond~~.

Claim 7 (Canceled)

Claim 8 (Currently Amended): The test method of a memory IC function, according to Claim 10 [[7]], wherein the random number is an arbitrary integer from 0 to 255.

Claim 9 (Canceled)

Claim 10 (Currently Amended): [[The]] A test method of a memory IC function, ~~according to Claim 9~~ comprising:

preparing a memory tester;

preparing ICs of different types;

transmitting data related to each test method of the ICs to the memory tester;

generating a random number;

executing a test of a predetermined IC based on the generated random number;

judging whether tests of all the ICs are finished or not;

repeating said generating a random number and said executing a test if tests of all the ICs are not finished; and

ending processing if tests of all the ICs are finished,

wherein the ICs include a memory IC, a communication interface IC, and a CPU peripheral IC, and wherein the memory IC includes Flash ROM, DRAM, and SDRAM.

Claim 11 (Currently Amended): The test method of a memory IC function, according to Claim 10 [[9]], wherein the communication interface IC is an IC including a UART interface and [[USB]] a universal serial bus interface.

Claim 12 (Currently Amended): [[The]] A test method of a memory IC function, ~~according to Claim 9~~ comprising:

preparing a memory tester;

preparing ICs of different types;

transmitting data related to each test method of the ICs to the memory tester;

generating a random number;

executing a test of a predetermined IC based on the generated random number;

judging whether tests of all the ICs are finished or not;

repeating said generating a random number and said executing a test if tests of all the ICs are not finished; and

ending processing if tests of all the ICs are finished,

wherein the ICs include a memory IC, a communication interface IC, and a CPU peripheral IC, and wherein the CPU peripheral IC is an IC including DMAC.

Claim 13 (Currently Amended): The test method of a memory IC function, according to Claim 10 [[7]], further comprising ~~a step of~~ performing timer interruption processing after said executing a ~~execution of the~~ test ~~of the memory IC~~.

Claim 14 (Currently Amended): The test method of a memory IC function, according to Claim 13, wherein the timer interruption processing is performed with a predetermined cycle. ~~The test method of a memory IC function, according to Claim 5, wherein~~

~~the predetermined cycle is defined by the millisecond~~[[.]]

Claim 15 (New): The test method of a memory IC function, according to claim 14, wherein the predetermined cycle is in a range of milliseconds.

Claim 16 (New): The test method of a memory IC function, according to Claim 12, wherein the random number is an arbitrary integer from 0 to 255.

Claim 17 (New): The test method of a memory IC function, according to Claim 12, wherein the communication interface IC is an IC including a UART interface and a universal serial bus interface.

Claim 18 (New): The test method of a memory IC function, according to Claim 12, further comprising performing timer interruption processing after said executing a test.

Claim 19 (New): The test method of a memory IC function, according to Claim 18, wherein the timer interruption processing is performed with a predetermined cycle.

Claim 20 (New): The test method of a memory IC function, according to claim 19, wherein the predetermined cycle is in a range of milliseconds.